N-Channel Enhancement Mode Power MOSFET

Description

The Power Device is produced using advanced TRENCH technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.
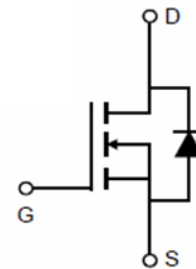
Features

- V_{DS}=60V , I_D=50A

- $R_{DS(ON)TYP} = 14m\Omega$ @ V_{GS} =10V

- Low gate charge (typical 33nC)

- High ruggedness

- Fast switching

- Good stability and uniformity with high EAS

- Improved dv/dt capability
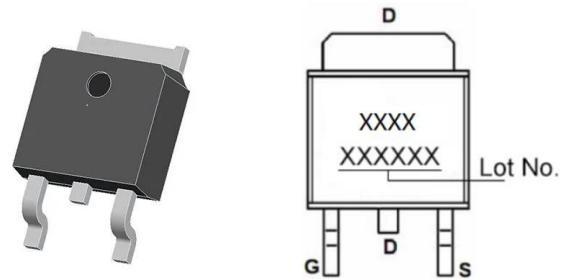
TO252-2L TOP VIEW

Marking and Pin Assignment

Schematic diagram

Applications

- DC/DC Converters in Computing, Servers

- Isolated DC/DC Converters in Telecom and Industrial

- Uninterruptible Power Supply

100% UIS TESTED!

100% ΔVds TESTED!

Package Marking and Ordering Information

Device Marking	Package	Packing	Reel (pcs)
SL50N06D	TO-252	Reel	2500

Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	± 30	V
Continuous Drain Current	T_C=25°C	I_D	50	A
	T_C=100°C		30	
Pulsed Drain Current(T_C=25°C,T_p Limited By T_{jmax}) (note1)		I_{DM}	200	A
Maximum Power Dissipation(T_C=25°C)		P_D	60	W
Avalanche energy , single Pulse(L=0.5mH) (note2)		E_{AS}	450	mJ
Peak Diode Recovery dv/dt (note3)		dv/dt	4.5	V/ns
Operating Junction And Storage Temperature		T_j,T_{stg}	-55 To 175	°C
Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		T_L	300	°C

Thermal Resistance

Parameter	Symbol	Max	Unit
Junction-to-Case	$R_{\theta JC}$	2.5	°C/W
Junction-to-Ambient	$R_{\theta JA}$	62.5	°C/W

Note:

1. Repetitive Rating : Pulse width limited by maximum junction temperature.

2. I_{AS}=50A, V_{DD}=50V, Rg=25Ω ,Starting T_J=25°C.

3. $I_{SD} \le$ 50A, di/dt $\le$ 200A/us, $V_{DD} \le BV_{DSS}$, Starting T_J = 25°C.

4. Pulse Test: Pulse Width $\le$ 300μs, Duty Cycle $\le$ 2%.

5. Essentially independent of operating temperature.
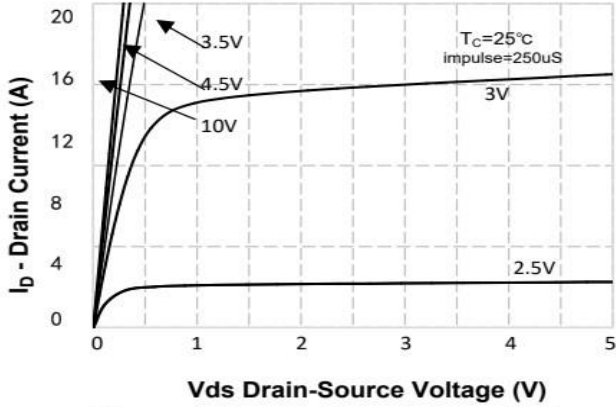
N- Channel Typical Characteristics

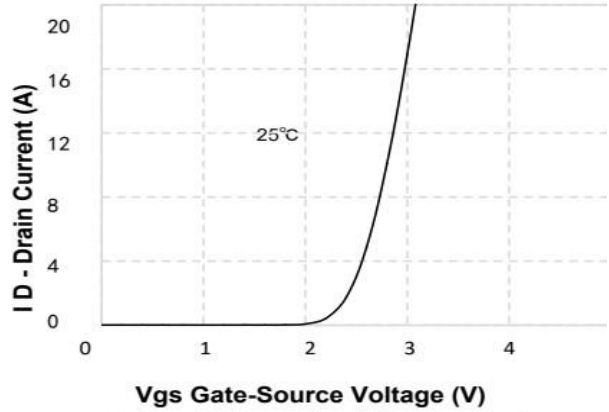Figure 1. On-Region Characteristics

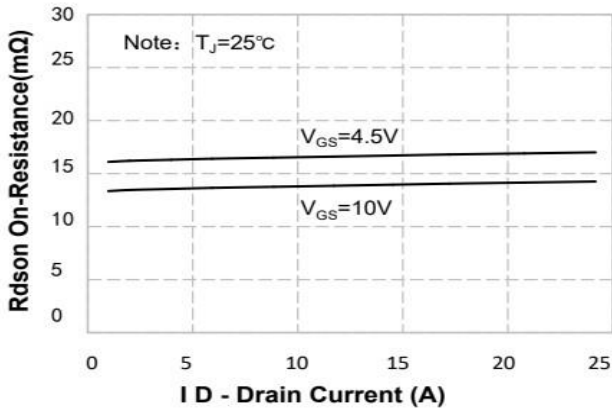
Figure 2. Transfer Characteristics

Figure 3. On-Resistance Variation vs
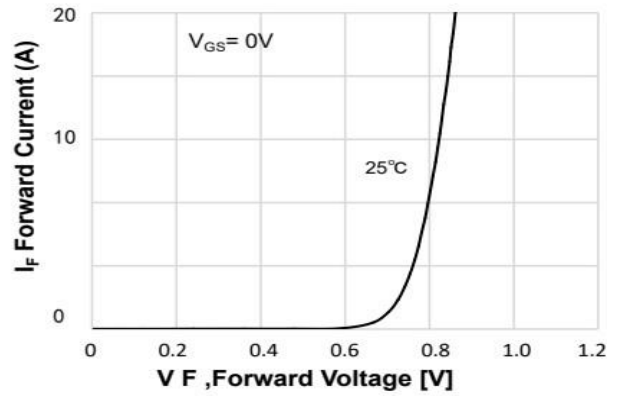Drain Current and Gate Voltage

Figure 4. Body Diode Forward Voltage
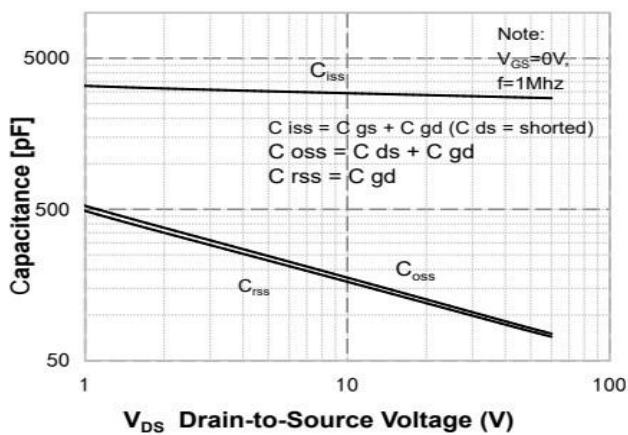Variation with Source Current
and Temperature
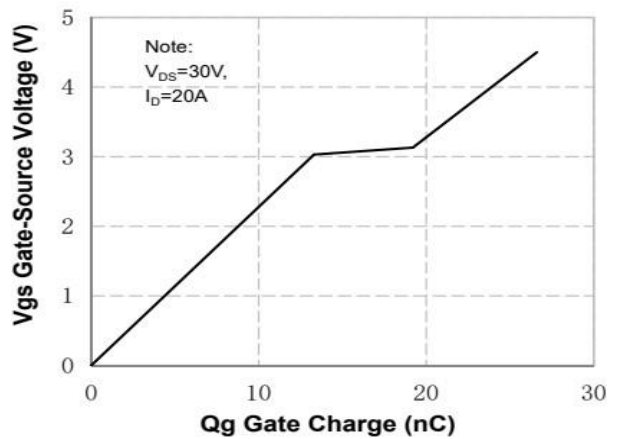

Figure 5. Capacitance Characteristics

Figure 6. Gate Charge Characteristics

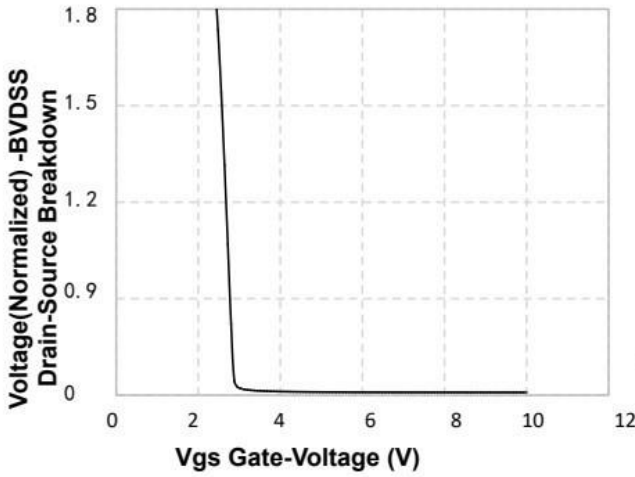## N- Channel Typical Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs Gate-Voltage

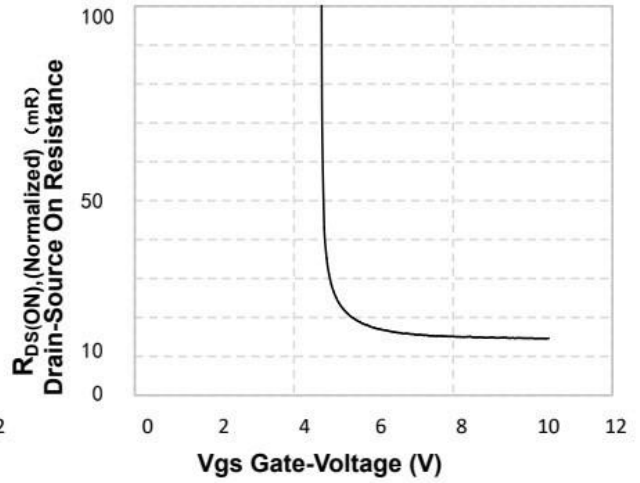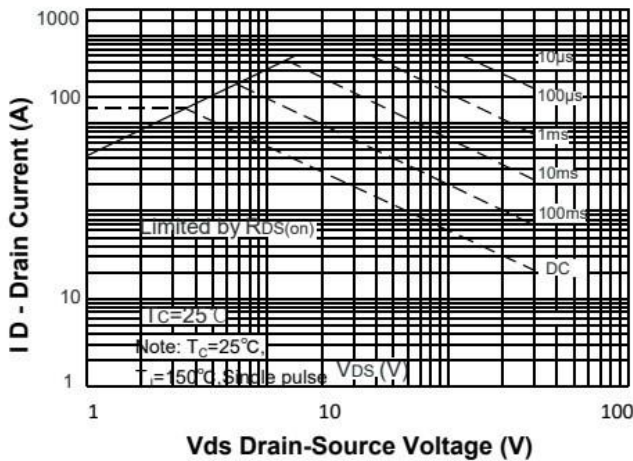Figure 8. On-Resistance Variation vs Gate Voltage
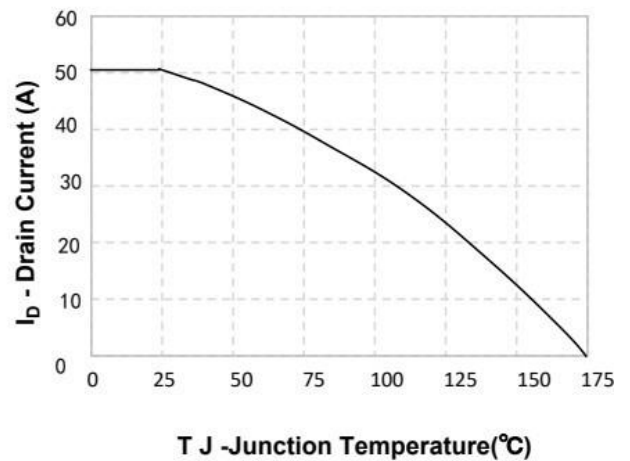

Figure 9. Maximum Safe Operating Area

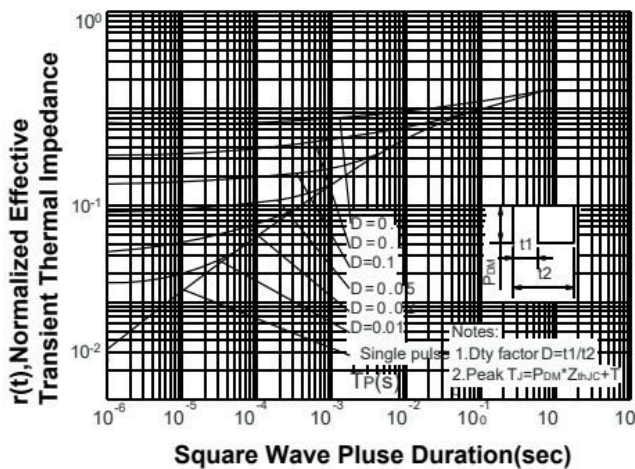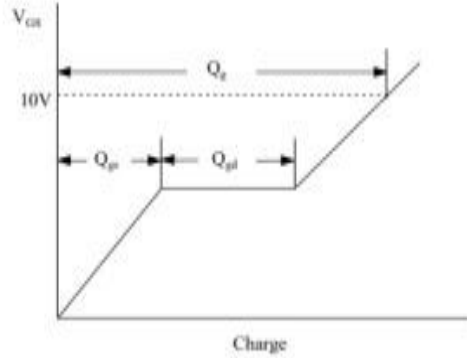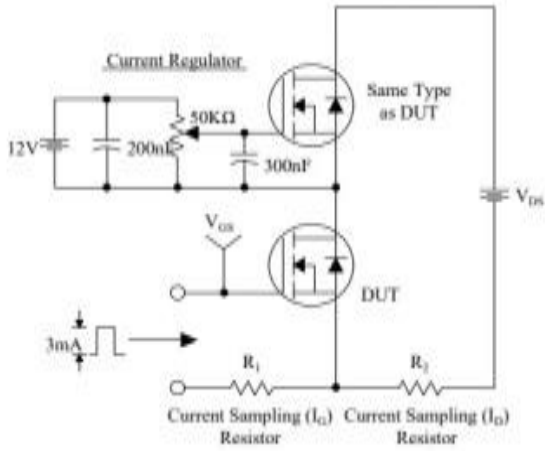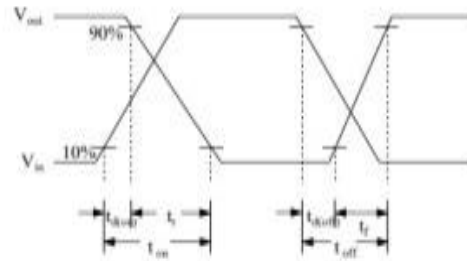Figure 10. Maximum PContinuous Drain Currentvs Case Temperature
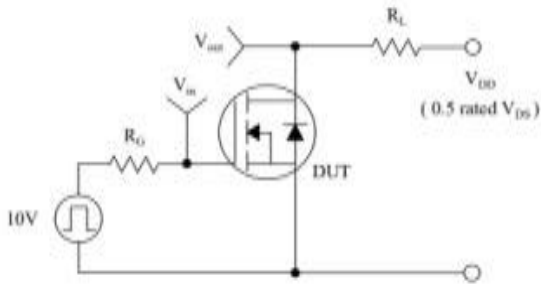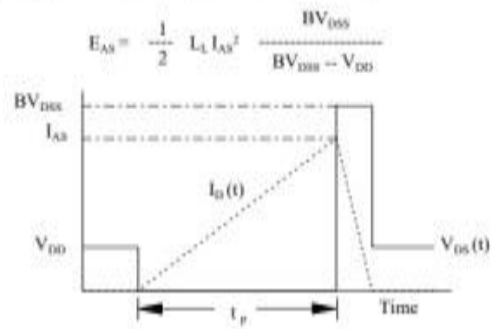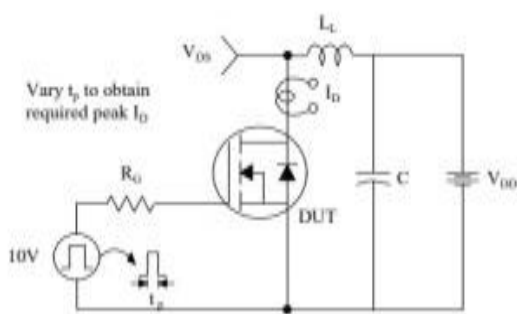

Figure 11. Transient Thermal Response Curve

Gate Charge Test Circuit & Waveform

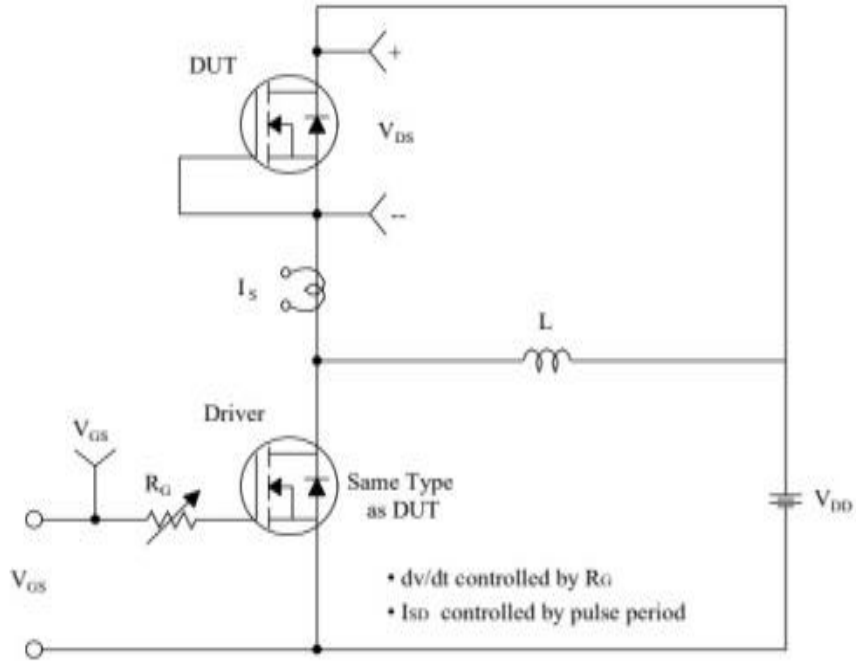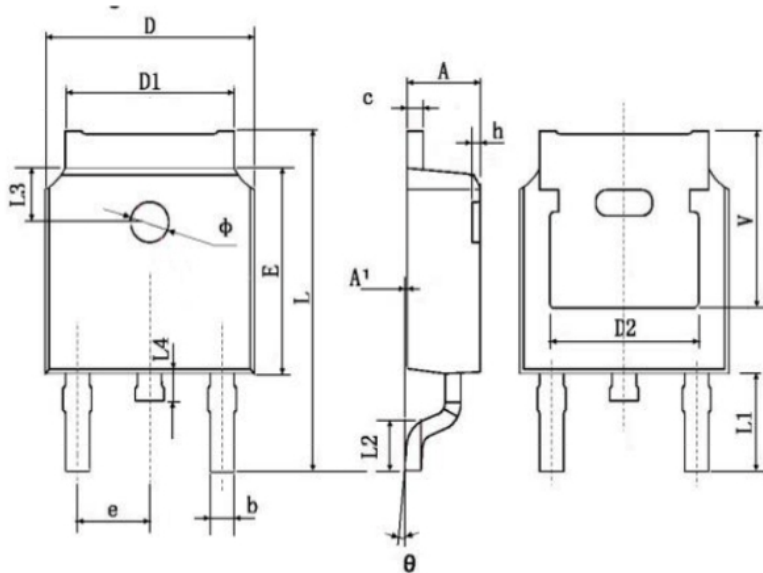## Resistive Switching Test Circuit & Waveforms

Unclamped Inductive Switching Test Circuit & Waveforms

$$E_{AS} = \frac{1}{2} L_L I_{AS}^2 \cdot \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

Peak Diode Recovery dv/dt Test Circuit & Waveforms
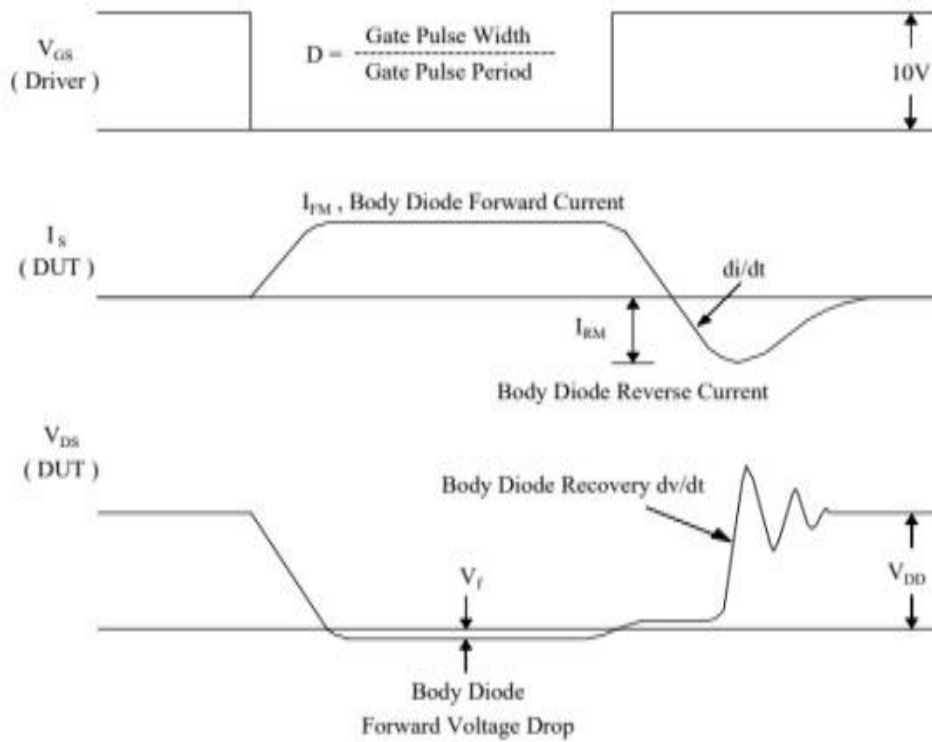
Package Information

TO-252   DPAK

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.250	2.350	0.089	0.093
A1	0.050	0.150	0.002	0.006
b	0.660	0.860	0.026	0.034
c	0.458	0.558	0.018	0.022
D	6.550	6.650	0.259	0.263
D1	5.234	5.434	0.207	0.215
D2	4.826 TYP.		0.191 TYP.	
E	6.050	6.150	0.239	0.243
e	2.236	2.336	0.088	0.092
L	9.820	10.220	0.388	0.404
L1	3.000 TYP.		0.119 TYP.	
L2	1.400	1.600	0.055	0.063
L3	1.800 TYP.		0.071 TYP.	
L4	0.700	0.900	0.028	0.036
Φ	1.150	1.250	0.045	0.049
θ	0°	3°	0°	3°
h	0.000	0.300	0.000	0.012
V	5.399 TYP		0.213 TYP	